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applying certain

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while building UVM
test benches,
which is mainly the
purpose of this
article. The Aim of
this Paper: 1. Focus
on the common
mistakes made by
the novice
engineers or
experienced users
while working on
UVM Methodology.
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2. TRICKS TO

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METHODOLOGY 2.1

Avoid using
uvm_config_db for
Replicating the
Changes between
Components. The
"uvm_config_db"
should not be used
to communicate
between different
components of the

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testbench when
the number of
variables becomes
too much. Instead
it's better to have a
common object.

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Tricks | Verification
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```
class  
serial_sequence  
extends
```

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```
uvm_sequence #(s  
erial_transaction);..  
.task body; if  
(starting_phase !=  
null) // UVM 1.1 sta  
rting_phase.raise_o  
bjection(this);  
repeat (count)  
begin @DUT_ready  
`uvm_do( trans )  
end if  
(starting_phase !=  
null) starting_phase  
.drop_objection(thi
```


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```
s); endtask  
endclass :  
serial_sequence.
```

Don't put DUT
timing into
sequence

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makefile.questa .
I would do this copy
makefile.questa as
Makefile .

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This tutorial
delivers a plethora
of tips and tricks to
alleviate the
struggle. It walks
you through an

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4.18 SystemVerilog
OVM or UVM

Library

Compilation.

Typically the OVM
or UVM libraries
are compiled using
directives like: +inc
dir+ /path/to/xvm/src
c. /path/to/xvm/src/
xvm_pkg.sv. Using
the -ovm or -uvm
directives. You can

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Use the `-ovm` or `-uvm` directives to compile the OVM or UVM libraries.

4.18 SystemVerilog OVM or UVM

Library Compilation

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then select Refactor > Migrate

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OVM to UVM. See
OVM to UVM
Migration

documentation
page for more
details. Add a new
file extension to
compile list ...

Chapter 42. Tips
and Tricks - DVT
Eclipse

2) to compile with
Modelsim use the

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makefile.questa . I
would do this copy
makefile.questa as
Makefile . Then do
gmake and it would
be fine . 3)If you
wanted to see the
compile command
do this . gmake -n
>run.csh . chmod
775
run.csh./run.csh [
We are just trying
to make a run

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script without any
makefiles] Hope
this works!

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UVM example? -
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Specific ...

I downloaded the
uvm package (UVM
1.1 (tar.gz) -
Accellera) from
verification
academy. While

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trying to compile the uvm code + u_first.sv I see the following error.

Compile command

used:-----vlog

-timescale

"1ns/1ns" -mfcu

-suppress 2181 +d

efine+UVM_NO_DPI

+acc=rmb

+incdir+uvm/src

uvm/src/uvm.sv

u_first.sv.

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UVM / OVM Other
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METHODOLOGY.

2.1 Avoid using
uvm_config_db for
Replicating the
Changes between

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Components. The
"uvm_config_db"
should not be used
to communicate
between different
components of the
testbench when
the number of
variables becomes
too much. Instead
it's better to have a
common object.

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and then become
productive with
UVM as quickly as
possible and to
reduce the burden
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code within a
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present Advanced
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randomize the item
or sequence. call
the start_item ()
and finish_item () if
its a uvm_sequenc
e_item object. call
the start () task if
its a sequence.

`uvm_do : execute
this sequence on

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default sequencer
with the item
provided.

``uvm_do_with` :
override any
default constraints
with inline values.

How to use

``uvm_do` sequence
macros

hi, all, Im a newer
in learning UVM.

With the support of

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many UVM experts, we can find many examples for learning UVM. However, when I tried to have a taste on some examples using VCS to compile them, the Makefile is a headache for me. Could you please let me know how to write a

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How to write a
good Makefile in
VCS for running
UVM tests ...

Press Shift + Alt +
Down Arrow to
restore the
previous selection
step made with
Shift + Alt + Up
Arrow. Format
source: Use the

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action from the editor right click menu Source > Format Source. The whole file is formatted or the current selection, if any. One key indentation: If you press Tab once at the beginning of a line, it is automatically

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